Prefetching Using Principles of Hippocampal-Neocortical Interaction

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Abstract

Memory prefetching improves performance across many systems layers. However, achieving high prefetch accuracy with low overhead is challenging, as memory hierarchies and application memory access patterns become more complicated. Furthermore, a prefetcher's ability to adapt to new access patterns as they emerge is becoming more crucial than ever. Recent work has demonstrated the use of deep learning techniques to improve prefetching accuracy, albeit with impractical compute and storage overheads. This paper suggests taking inspiration from the learning mechanisms and memory architecture of the human brain—specifically, the hippocampus and neocortex—to build resource-efficient, accurate, and adaptable prefetchers.

CCS Concepts

• **Computer systems organization → Architectures**; **Neural networks**; **Heterogeneous (hybrid) systems**; • **Computing methodologies → Bio-inspired approaches**.

Keywords

Prefetching, Memory Organization, Brain-Inspired Learning

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1 Introduction

Memory prefetching is a performance optimization used widely across several hardware and software layers of modern computer systems. Prefetching proactively brings data from slower levels of memory to faster ones, anticipating its future use. Although well-studied, prefetching continues to be explored, especially as emerging memory hierarchies embrace heterogeneity [22], disaggregation [27], vertical/horizontal tiering [31], and compute in memory [48].

Early prefetchers targeted patterns that were easy to capture, such as strides, and were sufficient for well-understood applications, such as those in SPEC [4]. However, systems and applications today are far more complex and dynamic, rendering simple approaches ineffective. There is a growing interest in developing prefetchers that can adapt to the dynamic execution by *learning* memory access patterns instead of detecting pre-programmed rules [11, 18, 40].

Recent studies have begun exploring the viability of deep learning (DL) for prefetching [11, 18, 30, 40]. In theory, DL should improve prefetching because it is inherently data-driven, and should naturally adapt to applications and their environments. Indeed, these studies show that, in idealized simulations, DL outperforms non-learning prefetch methods in accuracy. However, all of these approaches have three main shortcomings that impede their real-world adoption.

First, the deep neural networks (DNNs) in prior work use impractically high compute and storage resources, even as much as entire applications (§2.1). A more efficient and lightweight learning structure is crucial for real-world systems.

Second, prior approaches train their models offline, without learning continuously from the system execution. This is partly necessary due to the overhead of DNN training. However, such models can then fail to adapt to evolving application phases, configurations, inputs, and other system dynamics. Offline training also requires labeled datasets, which can be impractical to collect at scale.

Third, even if we were to optimize resource usage, online DNNs still face the challenge of catastrophic interference. This issue is well known in machine learning (ML) [23, 28], and describes the tendency of DNNs to drastically forget previously learned information when learning new information.

We consider the fundamental challenge of accurately learning memory access patterns online without interference. We argue that we can develop a robust solution by incorporating principles of learning found in the human brain. We note that the problem of learning access patterns is similar to a task that the human brain encounters continuously, which is to discover generalizable structure from its experiences.

In particular, we take inspiration from the cognitive theory of Complementary Learning Systems (CLS) [32], which models the human brain as an online learning system. CLS theory posits that the brain avoids catastrophic interference using *interleaved replay*, a process where it interleaves the learning of new and old information. Combining this insight with bio-inspired Hebbian networks, which use far less resources than DNNs, helps us build efficient, online prefetchers.

Many principles from CLS have already seen use in the ML community [13, 16, 44, 49]. Their objectives and constraints, however, differ from ours. In addition to maximizing model accuracy, we must further account for metrics like training and inference latency, prefetch timeliness, and usage of memory/network bandwidth. The combination of these constraints motivates a more domain-specific solution.

As we discuss how CLS principles can improve upon DL approaches, we also present expected implementation challenges with two real contexts: disaggregated systems [27] and CPU-GPU systems [3]. We specifically choose these because they experience high cross-node communication latency and operate in relatively resource-constrained settings. Thus, they stand to greatly benefit from intelligent memory prefetching. They also provide the opportunity to implement CLS principles in software, offering a faster path to immediate impact in production systems.

2 DL for Prefetching and Limitations

Prior DL techniques for cache or memory prefetching used transformers [30, 45] or Long Short-Term Memories (LSTMs) [18, 20, 40]. These DNNs use an application's recent cache/memory accesses and instructions to predict its next accesses, and have been shown to achieve high accuracy. However, they have unreasonable resource overheads and are only trained offline, thus remaining only simulated ideals.

Certain works have explored more lightweight learning algorithms for systems, such as reinforcement learning [11], gradient boosting [41], and small DNNs [24]. Unfortunately, these approaches too, were only evaluated in simulation, and we find in our testing that the lightweight models fail to match the prefetching accuracy of larger DNNs. Our goal is to develop online, accurate and resource-efficient prefetchers.

2.1 Overheads of DL-based Prefetching

DL-based prefetching incurs untenable compute and storage overheads. A state-of-the-art LSTM-based cache prefetcher [40] requires over 1 GB of storage using 32-bit parameters. This exceeds the memory capacity of some nodes in our target systems [27, 39]. We model this DNN for memory-page prefetching in a disaggregated system [27], and aggressively compress it to nearly 1 MB by reducing its input-embedding dimension, and the number of output classes. We compile this model on an Intel i7-8700 CPU, and measure its performance. We evaluate CPU performance because, for the inference times we target, which are around 1-10 μs [7, 27, 39], accelerator offloading is not clearly beneficial. Figure 1 shows the prefetcher's deployment.

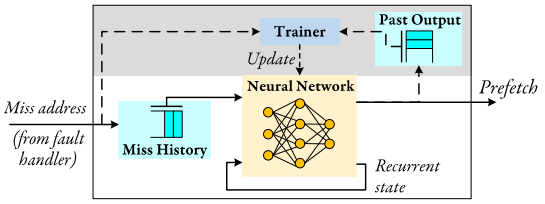
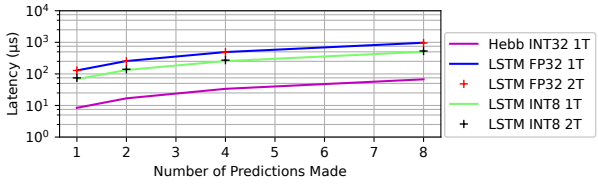
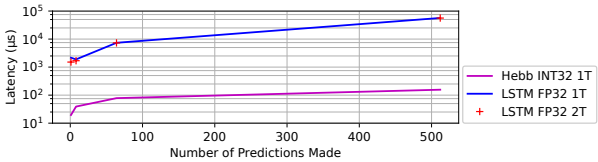


Figure 1: A DNN memory prefetcher. The gray area and dashed lines indicate steps during training.

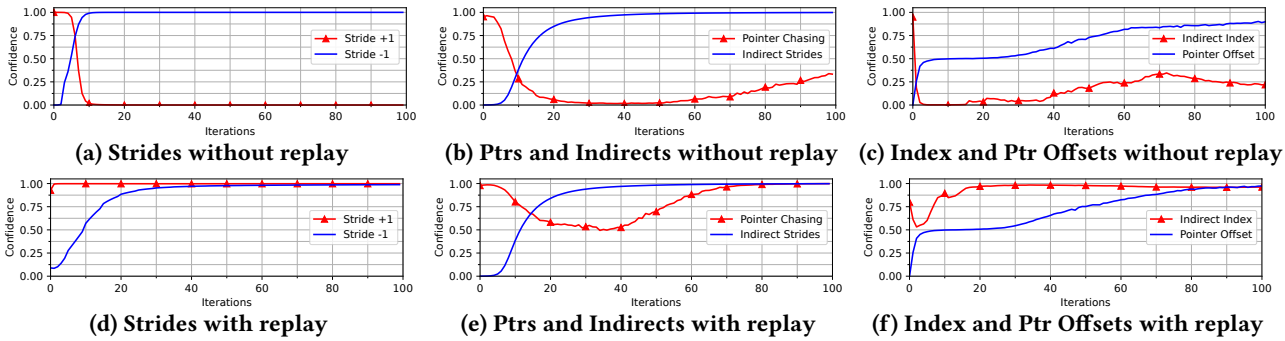


(a) Inference time for various number of future predictions.



(b) Training time for various batch sizes

Figure 2: Inference and training latency of a state-of-the-art LSTM prefetcher on an Intel i7-8700 CPU.



(a) Strides without replay (b) Ptrs and Indirects without replay (c) Index and Ptr Offsets without replay

(d) Strides with replay (e) Ptrs and Indirects with replay (f) Index and Ptr Offsets with replay

Figure 3: Catastrophic interference (a-c) and the effect of replay (d-f) during online prefetch learning. Confidence on the older pattern is shown in red, while the current one is in blue.

Figure 2 shows the LSTM latencies with one and two threads, and with parameter quantization (e.g., FP32 to INT8) during inference [29]. The LSTM takes >150 μs per inference and >1 ms per example for training, which are orders of magnitude higher than our target. Multi-threading is ineffective because LSTMs have poor parallelism [42]. Even after quantization, LSTM inference still takes >60 μs.

Table 1: Memory Access Patterns

Pattern	Code	Behavior
Stride	a[i]	Accessing data at regular delta such as streaming patterns or array traversal.
Pointer chase	*ptr	Pseudorandom accesses to different parts of the memory. E.g. linked list traversal
Indirect stride	*(a[i])	Accessing data at regular delta from a base address. E.g. array of object pointers.
Indirect index	b[a[i]]	Accessing data at indices that are at regular delta from a constant base address.
Pointer offset	*ptr *(ptr+i)	Pseudorandom accesses and adjacent data. E.g. transform on a list/tree.

2.2 Difficulty of Online Prefetch Learning

The scale of modern systems and dynamism of their applications makes it impractical to collect representative datasets with which DNN prefetchers can be trained offline. Instead, it is ideal if the model can adapt to changing memory access behavior by learning online. Unfortunately, learning online makes the DNN vulnerable to *catastrophic interference* [32].

Catastrophic interference occurs when a DNN trained on one pattern begins learning a different, unrelated pattern. The weight updates made when learning the new pattern overwrite the values that were critical in learning the older pattern, causing the DNN to completely forget the older one. Such interference is avoided during offline training by mixing training data and learning over it in multiple passes. This is not the case when learning online.

We use the LSTM from §2.1 to illustrate catastrophic interference with online prefetch learning. We first train the LSTM on a single memory access pattern (e.g., a constant stride) until it achieves perfect accuracy, simulating learning over a single application phase. Next, we present the LSTM with another access pattern (e.g., pointer chasing) to learn. We monitor the LSTM's confidence on the current and previous patterns, which is the probability it assigns to the correct prediction. We select different pairs of patterns from those in Table 1, adapted from prior work [10]. For a pair of patterns, we generate a trace of 1000 accesses with each pattern. We use these *data structure*-level prefetching patterns to avoid confounding effects possible in page-level prefetching.

Figures 3a-3c show our results. As the LSTM learns the current task, its confidence on the older task drops abruptly, demonstrating catastrophic interference. In some cases, the confidence on the first pattern recovers partially, indicating some knowledge transfer. Nonetheless, the final confidence is poor. Such a prefetcher will be ineffective when patterns repeat, which is the case with many applications.

3 Hippocampal-Neocortical Inspired Prefetching

Figure 4 shows the brain's learning architecture in CLS theory. Learning occurs through a complementary relationship between two regions of the brain: the neocortex and the hippocampus. The neocortex, similar to DNNs, slowly learns the structure underlying the information it encounters; i.e., the rules behind a memory access pattern. Meanwhile, the hippocampus quickly memorizes the information it encounters — i.e., the exact memory accesses — in a compressed format, likely by separating each access and storing them in an associative memory [35, 36]. Over time, this information is decompressed and replayed in the neocortex, interleaving the learning of old and new tasks, thus mitigating interference [25, 32]. Furthermore, CLS theory models the networks in the brain using biologically-inspired Hebbian networks, which have much lower resource needs compared to standard DNNs. We show how each of these ideas help overcome the limitations of standard DNNs for prefetching.

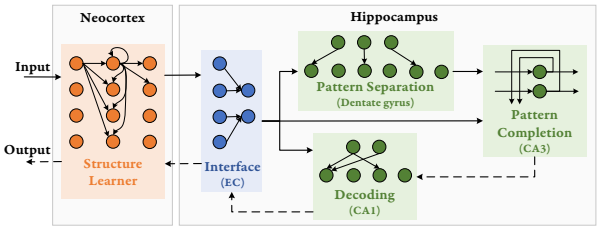


Figure 4: Memory architecture of the brain in CLS theory. Each block is modeled with a Hebbian neural network. Solid lines show information storage paths and dashed lines show recall and replay.

3.1 Overcoming Resource Overheads

Brain-inspired prefetch networks are resource efficient for two reasons. The first reason is that they use a Hebbian update rule, which is much simpler than that of standard DNN learning. When learning with Hebbian networks, a network weight w_{ij}—connecting an input neuron a_i and output neuron b_j—is increased if both neurons are non-zero, and decreased if the input neuron (a_i) is inactive while the output (b_j) is active. The simplified update rule [15, 36] is:

$$\Delta w_{ij} = (b_j \neq 0)[(a_i \neq 0) - (a_i == 0)] \quad (1)$$

This update scheme requires far fewer operations than conventional training of DNNs.

The second advantage of brain-inspired networks comes from their use of sparsity. These networks are sparse in their *connectivity*, meaning a node connects to only 1-25% of the nodes in adjacent layers unlike all-to-all connections in DNNs. Additionally, they are sparse in their *representations*, in that only 1-25% of the network's hidden layer neurons are activated on an input. As a result, the storage and compute needs of these networks are a fraction of those for DNNs.

We prototype a sparse Hebbian neural network for prefetching. The network has a single hidden layer of 1000 neurons, with 12.5% connectivity between layers, and 10% sparsity in the hidden layer. Like an LSTM, our network also uses a recurrent state to capture sequence memory.

Table 2 compares the resource needs of our Hebbian network with that of the LSTM from §2.2. We list the lower bound for the number of operations (Ops) in the LSTM, as its exact value varies with the implementation of transcendental functions (e.g., sigmoid and tanh). The Hebbian network is nearly 3× smaller than the LSTM with nearly an order of magnitude fewer Ops. Hence, the Hebbian training and inference times, shown in Figure 2, are proportionately lower.

Table 2: Resource Needs of Hebbian vs LSTM networks

Model	Parameters	#Ops (inference)	#Ops (training)
LSTM	170 k	> 170k FP	> 400k FP
Hebbian	49 k	14k INT	64k INT

We also compare the networks' prefetching accuracy with multiple applications that have various memory access patterns: TensorFlow [6] training ResNet-50 [19], PageRank [34] using GraphChi [26], mcf [4], and graph500 [1]. For each application, we collect a trace of 2 billion memory accesses and simulate them with a memory sized at 50% of the trace's footprint. We deploy both prefetchers as shown in Figure 1, with a miss history length of 1 input to the networks, and measure the percentage of misses removed compared to a baseline without prefetching. Figure 5 shows the results. Our network has comparable accuracy to the LSTM, even while consuming far fewer resources, showing the effectiveness of Hebbian learning.

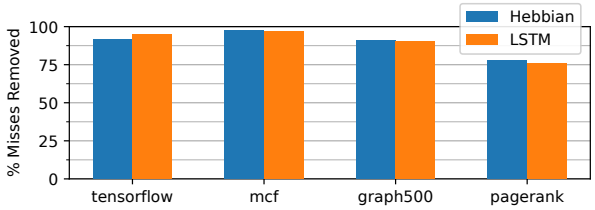


Figure 5: Online memory prefetching performance of Hebbian and LSTM networks.

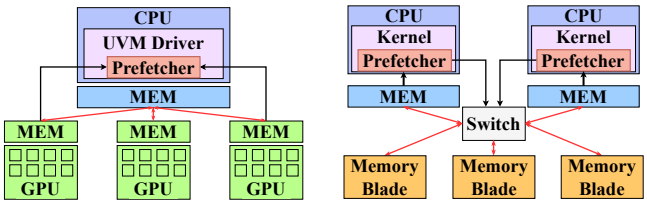
3.2 Overcoming Catastrophic Interference

In CLS theory, catastrophic interference is mitigated by *replaying* past memories stored in the hippocampus. Building a full hippocampal-like storage is an open problem requiring consideration on selectively storing and sampling accesses into it. Therefore, in this work, we will focus on showing the benefits of replay for online prefetch learning without resource limitations on the hippocampal storage.

We perform the experiments in §2.2 that showed catastrophic interference again, but with replay. We implement replay by retraining the network on the first pattern using a 0.1× smaller learning rate after each training/inference of the second. Figures 3d-3f shows the new results. While the models without replay experienced catastrophic interference, performing replay lets the network learn the new pattern *without forgetting* the old one. Even if the old pattern were to repeat, the network would maintain prediction accuracy without needing to re-learn it.

4 Target Systems for Online Prefetching

We target two environments for an initial deployment of our brain-inspired prefetcher: disaggregated systems [27] and CPU-GPU unified virtual memory (UVM) systems [3]. Both systems, shown in Figure 6, have data movement that incurs high communication latencies [7, 27], and stand to benefit from intelligent prefetching. However, the systems differ in a few critical ways that lead to requiring different types of prefetch strategies. One difference is the impact of a page miss. In disaggregated systems, CPU cores fault



(a) UVM system (b) Disaggregated system

Figure 6: Architectures of our target systems. Black lines indicate page miss notifications and prefetch requests. Red lines indicate data movement paths.

only on one page at a time, indicating that the prefetcher should be optimized to hide latency. In GPUs, the SIMT (single instruction multiple thread) execution can produce many concurrent faults, and the lockstep execution model means that a single fault can stall many threads. This suggests that a throughput-optimized prefetcher would be more appropriate for this system.

Our target systems also differ in the location from which the prefetchers can obtain information about memory accesses, and where the compute and memory resources to run prefetching are available. These parameters determine where the prefetcher should be placed. In the UVM system, software-level information on memory accesses is only available in the CPU-located driver. Therefore, all prefetching decisions must ultimately be made from this centralized location. This contrasts with the disaggregated system, where scarce resources on the switch necessitate a decentralized approach with a separate prefetcher per node.

The different placement of the prefetcher in each system, in turn, results in unique design spaces. For example, the prefetcher in the UVM system can take advantage of its global view to make better-informed decisions, but may require more processing to ensure that it can isolate the individual access patterns in the combined access streams. However, such interleaving of access streams may naturally offer more resistance to catastrophic interference, reducing replay costs.

In contrast, the prefetcher in the disaggregated system is less likely to see interleaved access streams since it has a separate prefetcher per CPU. Therefore, the prefetcher network could be smaller to learn the access patterns. With the decentralized architecture, it is easier to integrate application-specific, profile-guided prefetch optimizations.

5 Future Research Challenges

Our initials results with prefetchers based on the hippocampal-neocortical interaction are promising. Harnessing the full benefits of such a prefetcher requires solving important challenges to replicate the CLS architecture in Figure 4 in computer systems. We present these issues, beyond the target system-specific ones discussed in §4.

5.1 Training Instances

Training on every prefetch inference, as done in our experiments (§3.1), can be unnecessary and resource-consuming, especially because training is more expensive than inference. Possible alternatives are to train on a batch of samples at once, and/or to only train on certain misses. Training only on some misses reduces overall training costs, but requires care. Simple approaches, such as randomly deciding which samples to train on, may miss cases that are critical for the model to understand the application. A more intelligent sampling process could use confidence measures from the model to filter less-information carrying samples, or to avoid training on well-learned cases.

5.2 Prefetch Output and Miss History

There are two main parameters for the prefetcher's output: length, which is the number steps predicted into the future; and width, which is the number of predictions made at each step. The ideal values for these parameters are determined by the system architecture and application behavior. Consider our design from §3.1, where the network is trained only to predict the next miss. If the time between misses is less than the inference latency, even a perfect model will always prefetch too late. In that case, a more effective method is to predict a sequence of misses further into the future.

Regarding prefetch width, throughput-bound environments like the UVM system might benefit more from predicting multiple prefetches at a time, even if they have slightly less accuracy. The same could be said for read-heavy workloads. On the other hand, systems where the network is the bottleneck require a prefetcher that is highly selective and confident about bringing in data to minimize communication.

In order to learn how to predict with a given length and width, a prefetcher must maintain a miss history. For example, when prefetching multiple steps into the future, a window of past misses is required to construct appropriate training examples. Thus, the prefetch length determines a minimum history size. Beyond this, the ideal history size depends on the reuse distances in the access patterns of the application. If the current pattern has short reuse distances, then only a few entries in the miss history are necessary, while it is the opposite for patterns with longer reuse distances. Thus, configuring the prefetch length, width, and the access history will require intelligent co-design.

5.3 Encoding Data for Prefetching

Most prior work on ML-based prefetching encodes addresses and strides as one-hot vectors, which are then indexed into an embedding table to obtain a dense representation that is input to the prefetcher [18, 30, 40]. This aligns with approaches used for words in natural language processing, but storing

embeddings can become expensive (e.g., >500 MB [40]). It also inflates compute costs, as the output layer grows linearly with the number of embedding vectors.

A more fundamental issue is that addresses and strides can be a poor proxy for understanding the inherent behavior of an application. We found that, as of now, neither the LSTM nor the Hebbian network perform well on caching applications like memcached [17] and cachebench [12]. This is because these applications are almost entirely pointer-based, and the access patterns are difficult to learn from addresses or strides.

Ideally, the representation of the input data should more closely resemble how addresses "flow" at the data structure level (e.g. tree nodes, pointer chains). We have found that insights from the cognitive theories can provide inspiration here as well. There is evidence that the hippocampus encodes locations optimizing for vector-based navigation [33]. A similar encoding for addresses could better represent paths through data structures. Other brain-inspired work has explored ways of representing symbols that allow the efficient detection of relations in neural networks [8]. An analog of such an approach for prefetching would be an address embedding optimized for detecting pointers that are logically (as opposed to numerically) close to one another.

5.4 Implementing Replay

In our experiments to demonstrate the utility of replay, we assumed that we could store all past examples, and interleave them later. A full implementation must trade the storage/-compute costs of replay with its benefits for learning. One simple approach is to use a fixed-size buffer. This, however, could lose important information as entries are evicted. A more principled approach could save space by filtering less important examples, perhaps using confidence as a measure, or freeing entries that have already been consolidated due to replay, thus not needed further learning [32]. Yet another alternative is to average similar examples, producing single representative cases.

Another challenge in incorporating replay is to define application phases so that they can be replayed. However, phase characteristics can vary significantly between applications, making it difficult to manage replay with a single parameter setting (buffer size, time limits, miss counts, etc.). This could motivate an interface for application developers to directly tune replay parameters, or to indirectly indicate phase behavior and timings. Another approach, also inspired by cognitive theories, is to identify contexts or phases using clustering of abstract representations learned by the network [14].

Finally, our preliminary studies also show only one form of replay. Cognitive literature describes many forms of replay [46], each with their own benefits and challenges. Some methods such as *hindsight* or *simulation* replay, where the prefetcher artificially generates memory sequences and learns them, can be helpful in avoiding replay storage costs altogether. Such sequences could be generated by rules that are determined with profile-guided techniques, or through generative networks i.e., trading off compute for memory. Another alternative could generate hidden layer values, complete the forward pass, and train on the output to reinforce existing behavior. We leave such ideas for future research.

5.5 Availability

Since training actively changes the weights of a neural network, it may be important to block inference during training. This is an availability issue, which motivates a protocol where training is applied to a separate model copy, which is later redeployed when the live model's confidence/accuracy decreases. However, it is possible that simpler approaches could also suffice for two reasons. One, because prefetching is not correctness-critical, inference requests are safe to drop. Second, neural networks can have noise-robust or noise-smoothing effects, meaning that small perturbations to weights do not cause large changes in the network's output, especially since our training method explicitly seeks to preserve the network's prior performance [21, 35]. This could allow inference to remain accurate even when concurrent with training. We expect this property to require further study, as it could significantly optimize a real prefetcher deployment, but may be sensitive to the many details of practical implementation.

6 Conclusion

Recent deep learning approaches to prefetching have shown promising results, but only in idealized simulations. Their real implementation is impeded due to resource overheads and learning limitations. This paper explores how one might address these issues using principles and models of the hippocampus and neocortex, as well as some challenges we should expect in implementing them. We ultimately expect more challenges to appear in designing and deploying such models, but we hope this paper serves as a starting point for implementing efficient and intelligent learning algorithms for all relevant systems contexts.

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